Amendments to the Specification:

Please replace the paragraph beginning at page 21, line 10, with the following rewritten paragraph:

Another aspect of the present invention, is achieved by including the address translator in the register file or memory unit thereby creating a storage unit a programmer would view as a pool of register or memory locations that can be manipulated by operations on storage unit addresses. Consider an exemplary storage subsystem 800 of Fig. 8A, illustrating aspects of a read port, which operates differently than the storage subsystem 238 shown in Fig. 2D. In Fig. 8A, if the storage unit 810 is used as a register file for example, the address translation {s, e} bits would be considered architectural state information of the storage subsystem and the address translation is considered to be operative for each instructions accessed, as indicated by the {s, e} bits. In Fig. 2D subsystem 230, the address translation occurs only in operation for instructions that specify the address translation function. Other instructions, which don't specify an address translation function, use the register file or memory unit normally as sequentially addressed storage. In the storage subsystem 800 of Fig. 8A, all address inputs 815 are translated according to the translation settings 820 that govern how the addresses access data from the storage ~~unit~~ device 835. It is noted that port address latches may be included internal to the storage unit 810 at the outputs of the address translators or external depending upon application.